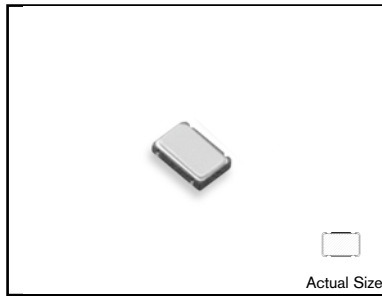


SERIES FMOCLVDSC2S3

2.5 Vdc LVDS Clock Oscillators

CERAMIC SMD 5x3.2



- Drives Fast LVDS Logic
- 2.5 Vdc Supply Voltage
- Complementary Output, Low EMI
- Reflow Soldering Temp. +260°C

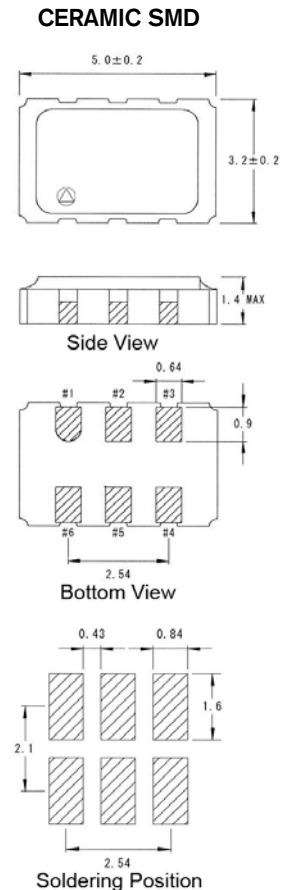


SPECIFICATIONS

issue 1 - 01252011

Parameter	Specification
Frequency Range	80.00 to 270.000 MHz
Overall Frequency Tolerance	±50 ppm standard, see options below (Inclusive of Operating Temp., Supply Voltage, & Load)
Operating Temperature Range	0°C to +70°C, -40°C to +85°C Available
Storage Temperature	-55°C to +125°C
Supply Voltage (Vdd)	+2.5 Vdc ± 5%
Supply Current (Icc)	66 mA max
Phase Jitter	0.3 pS RMS max Condition: 12 kHz to 20 MHz Band
Symmetry (Duty Cycle)	40/60%
Rise and Fall Time	0.7 nsec max
Output	LVDS
Output Load	100 ohms max (Offset 1.25V typical)
Output Signal	VOH: 1.43V typical VOL: 1.10V typical
Pin 1 Output Enable/Disable (note: do not connect to pin 1 if do not want this feature)	VIH: 0.7 Vcc min (Output Enabled) VIL: 0.3 Vcc max (Output: High Impedance) Enable Phase Delay Time 2ms max. Disable Phase Delay Time 200ns max.
Phase Jitter	0.3ps max (RMS, 12 kHz to 20 MHz)

Note: 0.01 µF external by-pass filter recommended.
All specifications subject to change without notice.



STANDARD MARKING

XXX.XXXM
• FMI YYWW

XXX.XXXM FREQUENCY in MHz
Pin 1 Symbol, FMI, Date Code

PIN FUNCTION TABLE

Pin	Function
1*	Enable/Disable (Tri-State)
2	NC
3	Ground
4	Output
5	Diff. Output
6	Supply Voltage (Vcc)

*Do not connect to Pin 1 if (tri-state) enable/disable is not required.

Standard Specifications for product indicated in color

Dimensions: $\frac{\text{Inches}}{\text{(mm)}}$

PART DESCRIPTION SYSTEM

